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EXAMINER	
TOLEDO, FERNANDO L	
ART UNIT	**PAPER NUMBER**
2823	

DATE MAILED: 09/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/673,214	SUZUKI ET AL.	
	Examiner	Art Unit	
	Fernando L. Toledo	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *20030930*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1 and 10 are rejected under 35 U.S.C. 102(e) as being anticipated by Machida et al. (US Patent Application Publication US 2003/0173601 A1).

In re claims 1 and 10, Machida, in the US Patent Application Publication US 2003/0173601 A1; figures 1 – 14 and related text discloses (a) preparing a semiconductor wafer 11 having a first principal plane on which an element is formed and a second principal plane opposite to the first principal plane; (b) forming a protective film 81 on the second principal plane only of the semiconductor wafer; (c) forming a gate insulating film 15 on the first principal plane, after the step (b); and (d) forming a conductor layer 16 on the gate insulating film (e) etching the conductive film to form a gate electrode.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 2 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Machida as applied to claims 1 and 10 above, and further in view of Wolf and Tauber (Silicon Processing for the VLSI Era Volume 1: Process Technology).

In re claims 2 and 11, Machida does not disclose wherein said gate insulating film in the step (c) is formed by subjecting said first principal plane to thermal oxidation, with said gate insulating film of said semiconductor wafer mounted on a support in first apparatus.

However, Wolf and Tauber, in the textbook Silicon Processing for the VLSI Era Volume 1: Process Technology, page 198, discloses that thermal oxidation is capable of producing SiO_2 films with controlled thickness and Si/SiO_2 interface properties.

It would have been obvious to one having ordinary skill in the art at the time the invention was made wherein said gate insulating film in the step (c) is formed by subjecting said first principal plane to thermal oxidation, with said gate insulating film of said semiconductor wafer mounted on a support in first apparatus in the invention of Machida, since, as taught by Wolf and Tauber thermal oxidation is capable of producing SiO_2 films with controlled thickness and Si/SiO_2 interface properties.

6. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Machida in view of Wolf and Tauber as applied to claims 1, 2, 10 and 11 above, and further in view of Kraft et al. (U. S. patent 6,136,654 A).

Machida in view of Wolf and Tauber discloses wherein said gate insulating film in the step (b) is formed by subjecting said first principal plane to thermal oxidation. However, Machida in view of Wolf and Tauber does not disclose and then to oxynitride processing the principal plane.

Kraft, in the U. S. patent 6,136,654 A; figures 1 – 7 and related text discloses forming an oxide layer on a semiconductor wafer and then oxynitride processing it to have a dielectric film substantially free of hydrogen (Abstract).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to oxynitride processing the layer of Machida and Wolf and Tauber, since Kraft teaches that an oxynitride process would free of hydrogen the dielectric layer.

7. Claims 3, 21 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Machida as applied to claims 1 and 10 above, and further in view of Maydan et al. (U. S. patent 5,882,165 A).

Machida discloses (d2) etching said conductive film into a predetermined pattern (Figure 6).

Machida does not teach (d1) mounting said semiconductor wafer on a support in second apparatus, so that said second principal plane having said protective film formed thereon comes in contact with the support, and forming a conductive film on said gate insulating film by using a

chemical vapor deposition method. However, Maydan, in the U. S. patent 5,882,165 A; figures 1 – 20 and related text, a multi-chamber apparatus wherein various semiconductor processes are preformed thereby providing the opportunity for multiple step, sequential processing using different processes in one system (Abstract).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to mounting said semiconductor wafer on a support in second apparatus, so that said second principal plane having said protective film formed thereon comes in contact with the support, and forming a conductive film on said gate insulating film by using a chemical vapor deposition method in the invention of Machida, since, as taught by Maydan, a multi-chamber apparatus various semiconductor processes can be preformed thereby providing the opportunity for multiple step, sequential processing using different processes in one system.

8. Claims 4 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Machida as applied to claims 1 and 10 above, and further in view of Hayashi et al. (U. S. patent 6,780,278 B2).

In re claims 4 and 12, Machida does not disclose said conductive film is selectively etched under a plasma atmosphere, to form said gate electrode. However, Hayashi discloses that plasma etching is a conventional process widely use in the semiconductor manufacturing processes (Column 1, Lines 17 – 19).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to use a plasma etching process with the invention of Machida, since, as

taught by Hayashi, plasma etching is a conventional process widely used in the semiconductor manufacturing processes.

9. Claims 5 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Machida as applied to claims 1 and 10 above, and further in view of Denning et al. (U. S. patent 6,187,682 B1).

In re claims 5 and 13, Machida does not teach comprising a step of cleaning said semiconductor wafer, after the step (b). However, Denning discloses, in the U. S. patent 6,187,682 B1; figures 1 – 10 and related text, that it is important to obtain atomically or near atomically clean substrate surfaces prior to formation of various films over the top of these surfaces (Column 1, Lines 15 – 18).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to clean the surface of the invention of Machida, since, as taught by Denning, it is important to obtain atomically or near atomically clean substrate surfaces prior to formation of various films over the top of these surfaces.

10. Claims 6, 7 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Machida as applied to claims 1 and 10 above, and further in view of Shih et al. (U. S. patent 6,589,852 B1).

In re claims 6, 7 and 14, Machida does not disclose forming a photoresist film pattern on said first principal plane of said semiconductor wafer, after the step (b) and before the step forming trenches for element isolation on said first principal plane, and using said photoresist

film pattern as a mask; removing said photoresist film pattern under a plasma atmosphere. However, Shih, in the U. S. patent 6,589,852 B1; figures 1 – 3 and related text discloses forming a photoresist film pattern on said first principal plane of said semiconductor wafer, after the step (b) and before the step forming trenches for element isolation on said first principal plane, and using said photoresist film pattern as a mask; removing said photoresist film pattern under a plasma atmosphere to form STI (Column 1, Lines 30 – 42) since STI is a preferred electrical isolation technique especially for a semiconductor chip with high integration (Column 1, Lines 30 – 33).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to form an STI structure in the invention of Machida, since as taught by Shih, STI is a preferred electrical isolation technique especially for a semiconductor chip with high integration.

11. Claims 8, 16, 21 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Machida as applied to claims 1 and 10 above, and further in view of Kawakubo Takashi (U. S. patent 6,242,298 B1).

In re claims 8 and 16, Machida does not disclose wherein said semiconductor wafer has a diameter of about 300 mm. However, Kawakubo, in the U. S. patent 6,242,298 B1; figures 1A – 23B and related text, discloses using wafers of 300 mm since with larger wafers denser semiconductor devices can be formed with a cheap product unit price (Column 9, Lines 36 – 40).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to form the device of Machida in a wafer of 300 mm in diameter, since as

taught by Kawakubo, with larger wafers denser semiconductor devices can be formed with a cheap product unit price.

12. Claims 9 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Machida as applied to claims 1 and 10 above, and further in view of Beauchaine et al. (U. S. patent 6,576,501 B1).

13. In re claims 9 and 17, Machida does not disclose wherein said first principal plane and said second principal plane of said semiconductor wafer in the step (a) have been subjected to mirror finishing. However, Beauchaine in the U. S. patent 6,576,501 B1; figures 1 – 4 and related text, discloses polishing the semiconductor wafer to a mirror-like polish to provide a smooth surface for manufacture (Column 1, Lines 45 – 48).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to subject the surfaces of the wafer of Machida to mirror-like finish, since as taught by Beauchaine polishing the semiconductor wafer to a mirror-like polish provides a smooth surface for manufacture.

14. Claims 18, 19, 21 and 26 – 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Machida in view of Denning.

In re claims 18, 21 and 28, Machida discloses (a) preparing a semiconductor wafer 11 having a first principal plane on which an element is formed and a second principal plane opposite to said first principal plane; (b) forming a protective film 81 on said second principal plane of said semiconductor wafer, with said first principal plane of said semiconductor wafer

placed on a support in first apparatus; (c) forming a metal or a metallic compound 16 on said first principal plane, after the step (b).

Machida does not teach (d) cleaning said second principal plane of said semiconductor wafer, after the step (c). However, Denning discloses, that it is important to obtain atomically or near atomically clean substrate surfaces prior to formation of various films over the top of these surfaces (Column 1, Lines 15 – 18).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to clean the surface of the invention of Machida, since, as taught by Denning, it is important to obtain atomically or near atomically clean substrate surfaces prior to formation of various films over the top of these surfaces.

15. In re claim 19, Machida discloses wherein the step (c) is a step of forming a copper film on said first principal plane (Figure 6).

16. In re claim 26, Machida discloses wherein the film is an insulating film formed by CVD method (Figure 6).

17. In re claim 27, Machida discloses wherein the insulating film includes an oxide film (Figure 6).

18. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Machida in view of Denning as applied to claims 18, 19, 21 and 28 above, and further in view of Shih.

Machida does not disclose wherein the copper film is formed by plating. However, Shih discloses various conventional ways to deposit copper such as plating (Column 6, Lines 43 – 51).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to form the copper layer of Machida by plating, since as taught by Shih, copper plating is a conventional way to form a copper layer in a semiconductor device.

19. Claims 22 – 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Machida in view of Denning as applied to claims 18, 19, 21 and 28 above, and further in view of Beauchaine et al. (U. S. patent 6,576,501 B1).

20. In re claims 22 – 25, Machida in view of Denning does not disclose wherein said first principal plane and said second principal plane of said semiconductor wafer in the step (a) have been subjected to mirror finishing. However, Beauchaine in the U. S. patent 6,576,501 B1; figures 1 – 4 and related text, discloses polishing the semiconductor wafer to a mirror-like polish to provide a smooth surface for manufacture (Column 1, Lines 45 – 48 and Abstract).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to subject the surfaces of the wafer of Machida to mirror-like finish, since as taught by Beauchaine polishing the semiconductor wafer to a mirror-like polish provides a smooth surface for manufacture.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fernando L. Toledo whose telephone number is 571-272-1867. The examiner can normally be reached on Mon-Thu 7am to 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

George Fourson
Primary Examiner
Art Unit 2823

FToledo
6 September 2004